REMARKS

Claims 1, 2, 4-7 and 9-36 are pending in the application.

Claims 1, 2, 4-7 and 9-36 have been rejected.

Claims 14, 27, 30 and 33-36 have been amended.

Claim 37 has been added.

Formal Matters

As an initial matter, Applicants would like to kindly thank the Examiner for clarification as to the typographical error in the earlier Office Action.

The specification is objected to for failing to provide proper antecedent basis for the claimed subject matter. Claims 33-35 have been amended to more clearly state the subject matter claimed, taking into consideration the spirit of the Examiner's comments and concerns. Applicants therefore respectfully submit that the specification need not be amended to address this issue, given the aforementioned amendments.

Rejection of Claims under 35 U.S.C. §101

Claims 33-35 stand rejected under 35 U.S.C. §101 because the claimed invention is directed to non-statutory subject matter. Claims 33-35 have been amended to more clearly state the subject matter claimed, taking into consideration the spirit of the Examiner's comments and concerns. Applicants therefore respectfully traverse this rejection.

Rejection of Claims under 35 U.S.C. §112

Claims 33-35 stand rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicant regards as the invention. Claims 33-35 have been amended to more clearly state the subject matter claimed, taking into consideration the spirit of the Examiner's comments and concerns. Applicants therefore respectfully traverse this rejection.

Rejection of Claims under 35 U.S.C. §102(b)

Claims 1, 4-7 and 9-36 stand rejected under 35 U.S.C. §102(b) as being anticipated by Kashima et al. (USPN 5,485,598) hereinafter referred to as ("Kashima"). Applicants respectfully traverse this rejection. Further, while not conceding that the cited reference qualifies as prior art, but instead to expedite prosecution, Applicants reserve the right, for example, in a continuing application, to establish that the cited reference, or other references cited now or hereafter, do not qualify as prior art as to an invention embodiment previously, currently, or subsequently claimed.

As generally recited in Applicants amended independent claims 14, 27, 30, 33, and 36, Applicants' independent claim 36, as amended, recites the following:

36. A method comprising:
maintaining a first cache, wherein
said maintaining is performed by one of an upper-level system and a lower-level storage module, and
said first cache is configured to provide read access and write access by said one of an upper-level system and a lower-level storage module;
cloning information stored in a first unit of storage into a second unit of storage, wherein
said first cache comprises said first unit of storage and a second cache comprises said second unit of storage; and
accessing said second cache, wherein
said accessing is performed by the other of said upper-level system and said lower-level storage module, and
said second cache is configured to provide read access and write access by said other of said upper-level system and said lower-level storage module.

Claims 14, 27, 30 and 33 have been amended similarly, and so include comparable limitations to claim one, among other of those claims limitations.

As can be seen, the independent claims now recite that the first cache is configured to provide read access and write access by one of an upper-level system and a lower-level storage module, while the second cache is configured to provide read access and write access by the other of these modules. Nowhere is there shown, taught or suggested in Kashima that the cache(s) disclosed therein, wherein any two systems can perform read and write operations to their respective caches.

Moreover, in light of this distinctions, Applicants once again respectfully submit that Kashima fails to show the cloning of the first cache into the second cache prior to modifying information in the first cache. The copying of Kashima (were such even comparable, which Applicants maintain it is not) differs markedly from the claimed cloning because neither of Kashima's first and second caches that are maintained by the upper-level system are accessible by a lower-level system (and certainly not in the claimed manner).

As amended, claim 36 recites other features not shown, taught or suggested by Kashima: "maintaining a first cache, wherein said maintaining is performed by one of an upper-level system and a lower-level storage module," "cloning information stored in a first unit of storage into a second unit of storage, wherein said first cache comprises said first unit of storage and a second cache comprises said second unit of storage," and "accessing said second cache, wherein said accessing is performed by the other of said upper-level system and said lower-level storage module." In particular, the cited portions of Kashima do not teach a system in which information is copied from a cache maintained by either an upper-level system or a lower-level storage module into another

cache, which is then accessed by the other one of the upper-level system or lower-level storage module.

In the Office Action, the Examiner equates the "upper-level system" of claim 36 with the CPU of Kashima, while also equating the "lower-level system" of the prior version of claim 36 with the OS of Kashima. Alternatively, the Examiner states that both the upper-level system and the lower-level system with computer 10 of Kashima.

Kashima, at best, teaches a system in which the old data cache can be part of the main memory system (e.g., as shown in Figs. 8 and 11 of Kashima) or part of a disk array (e.g., as shown in Figs. 4 and 14 of Kashima). Both the CPU and the OS are part of the computer 10. Neither the CPU nor the OS is a "lower-level storage module," as recited in the current version of claim 36. Computer 10 of Kashima is also clearly not a lower-level storage module. Accordingly, the cited art fails to teach or suggest the scenario claimed in amended claim 36, which involves a lower-level storage module maintaining or having access to a cache. And, as noted, even if such were the case (which Applicants do not concede), the read and write functionality provided by the claimed invention simply does not exist within Kashima.

In view of the above described distinctions as well as others, Applicants respectfully request the Examiner to withdraw the 35 U.S.C. § 102(e) rejection of independent claims 14, 27, 30, 33 and 36 as being anticipated by Kashima, and to recognize that newly added claim 37 is also not anticipated by Kashima. As dependent claims 3-13, 15-26, 28-29, 31-32, 34-35 and 37 add limitations to otherwise allowable base claims, Applicants urge the Examiner to withdraw the 35 U.S.C. § 102(e) rejection to these claims.

Rejection of Claims under 35 U.S.C. §103

Claim 2 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Kashima. Applicants respectfully traverse this rejection at least in light of the foregoing arguments.

Moreover, Applicants respectfully submit that the Office Action correctly states that Kashima fails to disclose anything comparable to the claimed first cache and the claimed second cache being portions of or the same cache. Applicants respectfully offer that such is the case at least for the reason that in the claimed architecture, such is not common knowledge or well-known in the art, and so do in fact traverse the Official Notice taken in the prior Office Action. Applicants' statement in this regard read:

> "Further with respect to claim 2, Applicant notes that, **regardless of whether it is well-known in the art to integrate certain types of caches, it is not well known to integrate caches such as those described in claim 2**. In particular, claim 2 describes a single cache that includes both a first cache and a second cache, the latter of which is maintained by either an upper-level system or a lower-level system and also able to be accessed by the other of the upper-level system or the lower-level system, as described in claim 36 (from which claim 2 depends). While the rejection addresses the general concept of combining two caches, no teachings or suggestions have been provided as to why one would integrate the two caches described in claim 36, which have specifically claimed functionality (e.g., the ability of the second cache to be maintained by one system while also capable of being accessed by another system)." (Office Action Response, dated February 1, 2007, p. 12; Emphasis supplied)

Thus, as can be seen, the Applicants never admitted to such being common knowledge or well-known (a point which Applicants in fact did not nor do not concede), but stated that even if such were the case (again, which Applicants did not nor do not concede), (1) Official Notice cannot be taken of the claimed single cache that includes both a first cache and a second cache because such a cache structure in the claimed architecture is not obvious (even in light of Kashima and/or any Official Notice so taken), and (2) that given the foregoing, Official Notice is not proper in such case, and Applicants therefore respectfully request the appropriate citation of a reference in this regard.

CONCLUSION

In view of the amendments and remarks set forth herein, the application and the claims therein are believed to be in condition for allowance without any further examination and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephone interview, the Examiner is invited to telephone the undersigned at 512-439-5084.

If any extensions of time under 37 C.F.R. § 1.136(a) are required in order for this submission to be considered timely, Applicant hereby petitions for such extensions. Applicant also hereby authorizes that any fees due for such extensions or any other fee associated with this submission, as specified in 37 C.F.R. § 1.16 or § 1.17, be charged to deposit account 502306.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Mail Stop Amendment, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on **August 23, 2007**.

Attorney for Applicants — Date of Signature: 8/23/07

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